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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRAN, THANH Y	

ART UNIT	PAPER NUMBER
2892	

MAIL DATE	DELIVERY MODE
12/23/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/801,208	LEE ET AL.	
	Examiner	Art Unit	
	THANH Y. TRAN	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-12,14,34-45 and 47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-7, 9-12, 14, 35-37, 47* is/are rejected.

7)☒ Claim(s) *8,34 and 38-45* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/6/09; 7/23/09; 11/19/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

In view of the Pre-Appeal Brief Review filed on 09/24/2009, PROSECUTION IS HEREBY REOPENED. The new ground(s) of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 2-4, 6, 9-12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimamoto et al. (U.S. 7,259,058) in view of Molla et al. (U.S. 2004/0175845).

As to claim 2, Shimamoto et al. disclose in figure 14(b) a method of fabricating a capacitor, the comprising: forming a lower electrode (comprising layers 22 and 23) on a substrate 11; forming a dielectric layer ("high-k dielectric film" 26) on the lower electrode (22, 23); and forming an upper electrode ("top electrode of ruthenium" 25) on the dielectric layer ("high-k dielectric film" 26) to provide a capacitor that comprises the lower electrode (comprising layers 22 and 23), the dielectric layer ("high-k dielectric film" 26) and the upper electrode ("top electrode of ruthenium" 25); wherein forming the lower electrode (comprising layers 22 and 23) on the substrate 11 comprises at least forming a ruthenium seed layer 22 on the substrate 11 and forming a main ruthenium layer ("bottom electrode of ruthenium" 23) on the ruthenium seed layer 22 using chemical vapor deposition ("CVD") (see col. 18, lines 21-26, the bottom electrode of ruthenium is formed by CVD processes).

Shimamoto et al. do not disclose a ruthenium seed layer is formed on the substrate by using atomic laver deposition ("ALD").

Molla et al. disclose in fig. 3 a method and a corresponding apparatus comprising: forming a ruthenium seed layer ("first seed layer" 20) on the substrate 12 by using atomic laver deposition (see paragraph [0011]). Therefore, it would have been obvious to a person having

ordinary skill in the art at the time the invention was made to modify the method of Shimamoto et al. by using atomic laver deposition for forming a ruthenium seed layer of the bottom/lower electrode on the substrate as taught by Molla et al. for controlling the composition easily with excellent step coverage.

As to claim 3, Shimamoto et al. disclose in figure 14(b) a method further comprising: forming a storage node contact plug ("plug 29 made of poly-si") on the semiconductor substrate 11 and a storage node ("polysilicon plug" 18) that is electrically connected to the storage node contact plug 29 to provide a semiconductor memory device, wherein the ruthenium seed layer 22 is formed on the storage node contact plug 29.

As to claim 4, Shimamoto et al. disclose in figure 14(b) a method of fabricating an electrode for a microelectronic device, the method comprising: forming a ruthenium seed layer 22 on a semiconductor substrate 11; forming a main ruthenium layer ("bottom electrode of ruthenium" 23) on the ruthenium seed layer 22; and patterning the main ruthenium layer 23 and the ruthenium seed layer 22 to form the electrode.

Shimamoto et al. do not disclose a ruthenium seed layer is formed on the substrate by using atomic laver deposition ("ALD"); and wherein forming the ruthenium seed layer using atomic layer deposition comprises injecting a ruthenium source into a chamber containing the semiconductor substrate.

Molla et al. disclose in fig. 3 a method and a corresponding apparatus comprising: forming a ruthenium seed layer ("first seed layer" 20) on the substrate 12 by using atomic laver deposition (see paragraph [0011]); and wherein forming the ruthenium seed layer 20 using atomic layer deposition inherently comprises injecting a ruthenium source into a chamber

containing the semiconductor substrate. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Shimamoto et al. by using atomic laver deposition for forming a ruthenium seed layer of the bottom/lower electrode on the substrate, wherein forming the ruthenium seed layer using atomic layer deposition inherently comprises injecting a ruthenium source into a chamber containing the semiconductor substrate as taught by Molla et al. for controlling the composition easily with excellent step coverage.

As to claim 6, Shimamoto et al. in view of Molla et al. do not disclose the oxygen-containing gas comprises an 02 gas, an 03 gas, and/or an H20 gas. However, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Shimamoto et al. in view of Molla et al. by using the oxygen-containing gas that comprises an 02 gas, an 03 gas, and/or an H20 gas for cleaning a low-temperature surface.

As to claim 9, Shimamoto et al. disclose in figure 14(b) a method of fabricating a capacitor, wherein the ruthenium seed layer 22 having a thickness of about 5 A to 50 A ("1nm to 2nm thick" of Ru seed layer 22 falls in the thickness range of 5A to 50 A).

Shimamoto et al. in view of Molla et al. do not disclose the main ruthenium layer having a thickness of 50 A to 300 A. However, the thickness range for a main Ru layer would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where

patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

As to claim 10, Shimamoto et al. in view of Molla et al. do not disclose supplying oxygen at a flow rate of about 1 sccm to 50 sccm for forming of the main ruthenium layer; and supplying a ruthenium source at a flow rate of about 0.1 ccm to 2 ccm under a pressure of about 0.4 Torr to 0.6 Torr. However, a flow rate of supplying oxygen of about 1 sccm to 50 sccm, or a flow rate of a ruthenium source about 0.1 ccm to 2 ccm under a pressure of about 0.4 Torr to 0.6 Torr would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

As to claim 11, Shimamoto et al. disclose in figure 14(b) a method of fabricating a capacitor, wherein the dielectric layer ("high-k dielectric film" 26) comprises a tantalum oxide layer ("tantalum pentoxide film") (see col. 17, line 57).

As to claim 12, Shimamoto et al. disclose in figure 14(b) a method of fabricating an electrode for a microelectronic device, the method comprising: forming a ruthenium seed layer 22 on a semiconductor substrate 11; forming a main ruthenium layer ("bottom electrode of

ruthenium" 23) on the ruthenium seed layer 22; forming a dielectric layer ("high-k dielectric" 26) on the main ruthenium layer ("bottom electrode of ruthenium" 23); and forming an upper electrode (comprising "top electrode of ruthenium" 25 and "top ruthenium seed layer" 24) on the dielectric layer 26 to provide a capacitor; wherein the main ruthenium layer ("bottom electrode of ruthenium" 23) is formed using chemical vapor deposition (see col. 18, lines 21-26, the bottom electrode of ruthenium is formed by CVD processes); wherein the forming of the upper electrode comprises: forming a second ruthenium seed layer ("top ruthenium seed layer" 24) on the dielectric layer 26; and forming a second main ruthenium layer ("top electrode of ruthenium" 25) on the second ruthenium seed layer 24.

Shimamoto et al. do not disclose a ruthenium seed layer is formed on a semiconductor substrate using atomic layer deposition; and a second ruthenium seed layer is formed on the dielectric layer using atomic layer deposition.

Molla et al. disclose in figs. 5-6 a method and a corresponding apparatus comprising: forming a first seed layer 20 on the substrate 12 by using atomic laver deposition; and forming a second seed layer 25 is formed on the dielectric layer 14 using atomic layer deposition (see paragraphs [0011] and [0016]). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Shimamoto et al. by using atomic laver deposition for forming first and second seed layers on the substrate and on the dielectric layer as taught by Molla et al. for controlling the composition easily with excellent step coverage.

As to claim 14, Shimamoto et al. disclose in figure 14(b) a method of fabricating an electrode for a microelectronic device, wherein the ruthenium seed layer has an oxygen concentration (see col. 5, lines 10-32).

Shimamoto et al. in view of Molla et al. do not disclose the oxygen concentration is less than 5%. However, applying a range of less than 5% for an oxygen concentration for controlling the thickness of the ruthenium seed layer would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

3. Claims 5, 7-8, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimamoto et al. (U.S. 7,259,058) in view of Molla et al. (U.S. 2004/0175845) as applied to claim 4 above, and further in view of Greer et al. (U.S. 7,107,998).

As to claims 5 and 7, Shimamoto et al. in view of Molla et al. disclose in fig. 3 purging the chamber inherently following the injection of the ruthenium source (see fig. 3 and paragraph [0011] in Molla et al.).

Shimamoto et al. in view of Molla et al. do not disclose the injection of the oxygen-containing gas, and the injection of the hydrogen-containing gas; and wherein at least one of the oxygen-containing gas or the hydrogen-containing gas is supplied in a plasma phase.

Greer et al. disclose in fig. 3 a method and a corresponding method comprising: the injection of the oxygen-containing gas, and the injection of the hydrogen-containing gas (see col. 11, line 48 – col. 12, line 20); and wherein at least one of the oxygen-containing gas or the hydrogen-containing gas is supplied in a plasma phase ("a remote plasma source") (see col. 2, lines 7-40). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Shimamoto et al. in view of Molla et al. by comprising the injection of the oxygen-containing gas and the injection of the hydrogen-containing gas, and wherein at least one of the oxygen-containing gas or the hydrogen-containing gas is supplied in a plasma phase as taught by Greer et al. for facilitating cleaning of ruthenium deposits on tubing walls at elevated temperature (see col. 11, line 48 – col. 12, line 20 in Greer et al.).

As to claim 8, Shimamoto et al. in view of Molla et al. and Greer et al. disclose injecting the ruthenium source, injecting the oxygen-containing gas, and injecting the hydrogen-containing gas into the chamber is performed until the ruthenium seed layer is grown to a desired thickness (see fig. 3, and col. 11, line 48 – col. 12, line 20 in Greer et al.).

Shimamoto et al. in view of Molla et al. and Greer et al. do not disclose injecting the ruthenium source, injecting the oxygen-containing gas, and injecting the hydrogen-containing gas into the chamber is performed at least twice. However, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method

of Shimamoto et al. in view of Molla et al. and Greer et al. by injecting the ruthenium source, injecting the oxygen-containing gas, and injecting the hydrogen-containing gas into the chamber at least twice for providing a desire thickness, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. See MPEP 2144.04.

As to claim 34, Shimamoto et al. in view of Molla et al. and Greer et al. do not disclose the hydrogen-containing gas is injected into the chamber after the oxygen-containing gas is injected into the chamber but before the ruthenium source is again injected into the chamber. However, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Shimamoto et al. in view of Molla et al. and Greer et al. by providing a change in sequent steps of injecting the gas into the chamber, since a change of sequences involves only routine skill in the art. See MPEP 2144.04

4. Claims 35-45 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimamoto et al. (U.S. 7,259,058) in view of Molla et al. (U.S. 2004/0175845) and Greer et al. (U.S. 7,107,998).

As to claims 35, 36, 37, and 47 Shimamoto et al. disclose in figure 14(b) a method of fabricating an electrode for a microelectronic device, the method comprising: forming a storage node contact plug (19, fig. 13a) on a semiconductor substrate 11; forming a ruthenium seed layer (22, fig. 14b) on the storage node contact plug (19, fig. 13a); and then forming a main ruthenium layer ("bottom electrode of ruthenium" 23) on the ruthenium seed layer 22; patterning the main ruthenium layer 23 and the ruthenium seed layer 22 to form the electrode; forming a dielectric layer ("high-k dielectric film" 26) on the electrode; forming an upper electrode ("top electrode of

ruthenium" 25) on the dielectric layer 26 to provide a capacitor; and inherently purging the chamber following the injection of the ruthenium source.

Shimamoto et al. do not disclose forming a ruthenium seed layer using atomic layer deposition ("ALD") by injecting a ruthenium source into a chamber containing the semiconductor substrate.

Molla et al. disclose in fig. 3 a method and a corresponding apparatus comprising: forming a ruthenium seed layer ("first seed layer" 20) using atomic laver deposition (see paragraph [0011]) by inherently injecting a ruthenium source into a chamber containing the semiconductor substrate. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Shimamoto et al. by forming a ruthenium seed layer using atomic layer deposition ("ALD") by injecting a ruthenium source into a chamber containing the semiconductor substrate as taught by Molla et al. for controlling the composition easily with excellent step coverage.

Shimamoto et al. in view of Molla et al. do not disclose the injection of the first oxygen-containing gas into the chamber containing the semiconductor substrate, and then injection a second hydrogen-containing gas that is different than the first oxygen-containing gas into the chamber containing the semiconductor substrate, wherein the first oxygen-containing gas comprises an 02 gas, an 03 gas, and/or an H20 gas and the second hydrogen-containing gas comprises an H2 gas and/or an NH3 gas, and the second hydrogen-containing gas does not include oxygen.

Greer et al. disclose in fig. 3 a method and a corresponding method comprising: the injection of the first oxygen-containing gas into the chamber containing the semiconductor

substrate, and then injection a second hydrogen-containing gas that is different than the first oxygen-containing gas into the chamber containing the semiconductor substrate, wherein the first oxygen-containing gas comprises an 02 gas, an 03 gas, and/or an H20 gas and the second hydrogen-containing gas comprises an H2 gas and/or an NH3 gas (see col. 9, lines 4-50); and wherein the second hydrogen-containing gas does not include oxygen (see col. 11, line 48 – col. 12, line 20). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Shimamoto et al. in view of Molla et al. by comprising the injection of the first oxygen-containing gas into the chamber containing the semiconductor substrate, and then injection a second hydrogen-containing gas that is different than the first oxygen-containing gas into the chamber containing the semiconductor substrate; wherein the first oxygen-containing gas comprises an 02 gas, an 03 gas, and/or an H20 gas and the second hydrogen-containing gas comprises an H2 gas and/or an NH3 gas; and the second hydrogen-containing gas does not include oxygen as taught by Greer et al. for facilitating cleaning of ruthenium deposits on tubing walls at elevated temperature (see col. 11, line 48 – col. 12, line 20 in Greer et al.).

As to claims 38 and 39, Shimamoto et al. in view of Molla et al. and Greer et al. disclose the method, wherein at least one of the oxygen-containing gas or the hydrogen-containing gas is supplied in a plasma phase ("CVD"/"ALD"); and wherein the main ruthenium layer is formed using chemical vapor deposition (see col. 9, lines 4-50; col. 11, line 48 - col. 12, line 20 in Greer et al.). It should be noted that: "CVD"/"ALD" process inherently converts to plasma phase.

As to claim 40, Shimamoto et al. in view of Molla et al. and Greer et al. disclose injecting the ruthenium source, injecting the oxygen-containing gas, and injecting the hydrogen-containing

gas into the chamber is performed until the ruthenium seed layer is grown to a desired thickness (see fig. 3, and col. 11, line 48 – col. 12, line 20 in Greer et al.).

Shimamoto et al. in view of Molla et al. and Greer et al. do not disclose injecting the ruthenium source, injecting the oxygen-containing gas, and injecting the hydrogen-containing gas into the chamber is performed at least twice. However, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Shimamoto et al. in view of Molla et al. and Greer et al. by injecting the ruthenium source, injecting the oxygen-containing gas, and injecting the hydrogen-containing gas into the chamber at least twice for providing a desire thickness, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. See MPEP 2144.04.

As to claim 41, Shimamoto et al. disclose in figure 14(b) a method of fabricating an electrode for a microelectronic device, wherein the ruthenium seed layer has an oxygen concentration (see col. 5, lines 10-32).

Shimamoto et al. in view of Molla et al. and Greer et al. do not disclose the oxygen concentration is less than 5%. However, applying a range of less than 5% for an oxygen concentration for controlling the thickness of the ruthenium seed layer would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim,

the Applicant must show that the chosen dimensions are critical. See In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

As to claim 42, Shimamoto et al. disclose in figure 14(b) a method of fabricating a capacitor, wherein the ruthenium seed layer 22 having a thickness of about 5 A to 50 A ("1nm to 2nm thick" of Ru seed layer 22 falls in the thickness range of 5A to 50 A).

Shimamoto et al. in view of Molla et al. and Greer et al. do not disclose the main ruthenium layer having a thickness of 50 A to 300 A. However, the thickness range for a main Ru layer would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

As to claim 43, Shimamoto et al. in view of Molla et al. and Greer et al. do not disclose supplying oxygen at a flow rate of about 1 sccm to 50 sccm for forming of the main ruthenium layer; and supplying a ruthenium source at a flow rate of about 0.1 ccm to 2 ccm under a pressure of about 0.4 Torr to 0.6 Torr. However, a flow rate of supplying oxygen of about 1 sccm to 50 sccm, or a flow rate of a ruthenium source about 0.1 ccm to 2 ccm under a pressure of about 0.4 Torr to 0.6 Torr would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected

results, it is not inventive to discover optimal or workable ranges by routine experimentation. In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

As to claim 44, Shimamoto et al. disclose in figure 14(b) a method of fabricating a capacitor, wherein the dielectric layer ("high-k dielectric film" 26) comprises a tantalum oxide layer ("tantalum pentoxide film") (see col. 17, line 57).

As to claim 45, Shimamoto et al. disclose in figure 14(b) a method of fabricating an electrode for a microelectronic device, the method comprising: forming of the upper electrode comprises: forming a second ruthenium seed layer ("top ruthenium seed layer" 24) on the dielectric layer 26; and forming a second main ruthenium layer ("top electrode of ruthenium" 25) on the second ruthenium seed layer 24.

Shimamoto et al. do not disclose a second ruthenium seed layer is formed on the dielectric layer using atomic layer deposition.

Molla et al. disclose in figs. 5-6 a method and a corresponding apparatus comprising: forming a second seed layer 25 is formed on the dielectric layer 14 using atomic layer deposition (see paragraphs [0011] and [0016]). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Shimamoto

et al. by using atomic laver deposition for forming second seed layer the dielectric layer as taught by Molla et al. for controlling the composition easily with excellent step coverage.

Response to Arguments

5. Applicant's arguments with respect to claims 2-12, 14, 34-45 and 47 have been considered but are moot in view of the new ground(s) of rejection.

With respect to the previous amended claims 2-12, 14, 34-45 and 47 filed on 07/14/2008, the new ground(s) of rejection as set forth above.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le, can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/T. Y. T./
Examiner, Art Unit 2892

/Thao X Le/
Supervisory Patent Examiner, Art Unit 2892